CLAIMS

1. A hybrid computer comprising at least one cell having at least one integrator circuit (1) in which time dependent input voltage is applied through at least one input resistance and its sign is changed after the integration, at least one cell having at least one analog integrator circuit (2) in which the input voltage is applied to the inverting input of Opamp (302) to change sign, then applied to at least one resistor, at least one cell having at least one coordinator circuit (6) and at least one analog integrator circuit connected to said coordinator circuit (6), a micro controller and a digital computer (7) including a data acquisition system, said hybrid computer characterized in that;
   i. Analog integrator circuits (1,2) interconnected over coordinator circuits(6) that perform synchronized and time continuous integration.
   ii. Disconnection of all analog integrators from each other at required time intervals, loading of the magnified error voltage that occurs when the input voltage of the Opamp's is set to zero, in the memory included in the integrator circuits (1,2).
   iii. As the analog integrator circuits (1,2) are interconnected again, demagnifying the error voltages that are loaded in the memories, by the same ratio of magnification applied during loading and use it to eliminate error during integration.
   iv. Data transferring from analog circuits to digital computer (7) at desired intervals and displaying the results after processing.

2. The coordinator circuit (6) of Claim 1 executing operations such as summation, subtraction of variable voltages, multiplication by a constant, division by a constant and integration having output voltages as feedback to other analog integrator circuits through the analog integrator circuit connected to said coordinator circuit (6).

3. An analog integrator circuit according to Claim 1 wherein an operation amplifier (Opamp) (301) having an inverting and a non-inverting input, that provides an output voltage that is fed back via a resistor (401) to said inverting input, when the said non-inverting input is grounded, output voltage (error voltage) of the said amplifier is applied by magnifying to inverting input of another Opamp also having

a non-inverting input through a resistor (403), the output voltage of this Opamp is fed back via another resistor having a same resistance to said inverting input, the output voltage of said opamp is loaded to a capacitor (501).

4. An analog integrator circuit (1) according to Claim 3 wherein input voltage is a function of time is applied to the inverting input of Opamp (301) through at least one input resistor R(τ) (404) when non-inverting input of said Opamp (301) is not grounded, output of said Opamp (301) is connected to a Capacitor (502) and in turn said Capacitor (502) is connected to input resistor R(τ) (404), the voltage loaded to a Capacitor (501) when non-inverting input of said Opamp (301) is grounded by magnified is applied to non-inverting input of Opamp (301) through a resistor (401) by means of a switch (105) by demagnifying by the amount magnified and the results of integration are transferred to a coordinator circuit (6).

5. An analog integrator circuit (2) according to Claim 3 wherein input voltage as a function of time is applied to the inverting input of Opamp (302) also having a non-inverting input through a resistor (403), output voltage of said opamp is fed back via another resistor (403) having same resistance with said resistor (403) to said inverting input of said opamp (302), output voltage of said Opamp with opposite sign is applied to inverting input of another Opamp (301) having an inverting and a non-inverting input through at least one input resistor R(τ) (404), the output of said Opamp (301) is connected to a capacitor (502) and in turn said capacitor (502) is connected to input resistor (404), voltage loaded to the capacitor (501) when non-inverting input of said Opamp (301) is grounded by being magnified is applied by demagnifying to non-inverting input of Opamp (301) through a resistor (401) by means of a switch when non-inverting input of said Opamp (301) is not grounded and the results of integration are transferred to a coordinator circuit (6).

6. A hybrid computer of Claim 1 comprising a circuit wherein output voltage of Opamp (307) having an inverting and a non-inverting input is fed back via a resistor (417) to said inverting input of said Opamp when non-inverting input of said Opamp (307) is grounded, output voltage of said Opamp (307) is loaded to a capacitor (503) by being magnified and reference leg of said capacitor (503) is connected to non-inverting input of said Opamp (307).

7. A circuit (5) according to Claim 6 wherein input voltage as a function of time is applied to non-inverting input of Opamp (307) having an inverting and a non-inverting input through at least one resistor (420), voltage loaded to a capacitor (503) before by being magnified is applied to inverting input of said Opamp (307) by demagnification with same ratio.

8. A computer according to Claim 1 wherein error voltage is loaded to analog memory.

9. A computer according to Claim 1 wherein error voltage is loaded to digital memory.

10. A circuit according to Claim 3 wherein initial conditions are loaded to the capacitor (502) connected to the input resistor (404).

11. A circuit according to Claim 5 wherein initial conditions are loaded to the capacitor (502) connected to the input resistor (404).

12. A computer according to Claim 1 wherein results of integration are transferred time continuously to a digital computer (7)

13. A computer according to Claim 12 wherein results of integration are transferred continuously to a digital computer (7) by at least one micro controller.

14. A computer according to Claim 1 comprising at least one programmable micro controller.